Remarks

Specification

Page 11 was corrected to correct the typographical error introduced by the printer. No new matter was introduced by the correction since semiconductor dimensions all fall into the μm range as is commonly known in the art. It would therefore have been clear to any person skilled in the art that the various depths to the n-well, p+emitter and n+region, by necessity, had to refer to depths in μm.

Rejection under 35 USC 112, second paragraph:

Independent claim 1 has been amended to simplify the language by referring to a reduction in size as compared to a conventional LVTSCR. (The second region refers to p+ emitter region 316 in Figure 3, as is clear from the specification and Figure 3) The deleted wording merely sought to describe the internal mechanism involved in achieving the increase in holding voltage. Since this is not relevant to the structural details of the device, the claim has been amended to include only structural details necessary to achieve the desired result.

Support for this change can be found on page 8, first and second paragraphs of Detailed Description of the Invention. Thus no new matter is added by this change. (For purposes of this response the emitter region that is reduced in size in accordance with the invention will be referred to as the p+emitter region. However, it will be appreciated that the polarity depends on the nature of the embodiment, as is discussed in the last paragraph on page 11.)

It is respectfully submitted that Claim 1 as previously claimed and as now amended is not indefinite under 35 USC 112.

Amended Claims 1 specify the size relative to a prior art device. They have further been amended to specify that the prior art device refers to a device that uses the same process.

It would not make sense to define the sizes or regions as an absolute value instead of by reference to the context. Sizes of regions in a semiconductor structure vary depending on the process adopted. For, instance gate, drain and source sizes in a GGNMOS will vary depending on whether a 0.18 micron process was used as opposed to a 0.25 micron process, for example.

Furthermore, the present invention does not propose any one particular size for the p+ emitter region. What is important in the present invention is that it provides a new approach and the flexibility to create a device with the desired holding voltage or that supports the desired current densities needed for a particular application. Depending on the application for which the device is to be used, different holding voltage or current density parameters may be needed. By using the approach of the present invention, of adjusting the size of the p+ emitter region and the n+ emitter region, the holding voltage and current density can be adjusted. Knowing what holding voltage and current density is required for a particular application, it is a simple technique, to then determine the necessary sizes of the structures using simulation results, e.g., TCAD simulations.

As mentioned in the background to the invention, GGNMOS typically suffers from low current densities, while LVTSCRs, in turn, suffer from the problem of low holding voltage. By reducing the size of the p+ emitter region in a LVTSCR-like structure to varying degrees, device parameters can be achieved that fall anywhere between a LVTSCR and a GGNMOS. This is most clearly illustrated in Figure 6 in which one embodiment of a LVTSCR-like structure (curve 62) of the present invention is compared to a standard GGNMOS (curve 64). This particular embodiment of the invention provided much the same holding voltage as the GGNMOS but, as mentioned on page 11, second paragraph, and as shown by the curves, it provided much high current in the on-state (approximately three times greater). Thus the techniques of the invention allows a device to be created that displays high current capabilities (similar to a conventional LVTSCR) while achieving high holding voltages similar to a GGNMOS device. It will also be appreciated that a whole range of parameters falling between those of GGNMOS and conventional LVTSCR can be achieved using the method of the present invention.

From the discussions on page 11, second paragraph, and Figure 5, it will be appreciated that the present invention does not contemplate any one particular size to the p+ emitter – it contemplates improving the holding voltage and current density by manipulating the size of the p+emitter. In the examples given, the p+ emitter was chosen to have lengths ranging from 0.6 to 2.5 μm. As can be seen from Figure 5, the holding voltage increased as the size of the p+region decreased.

Claims 2 and 3 are dependent from new claim 1 and therefore include the same limitations and are therefore also sufficiently definite in terms of 35 USC 112.

Claim 3 has been amended to specify that the third region is increased in size relative to the corresponding region in a conventional LVTSCR device. (The effect of increasing the size of the third region (n+region 322) is explained on page 8, last two lines, read with last 4 lines of page 9 and first 4 lines of page 11. Increasing n+ region 322 provides more electrons relative to the holes injected by region 316)

Again, it is respectfully submitted that specifying the size relative to the prior art device makes the claim sufficiently definite. Furthermore, no new matter is introduced by this information since n+ region sizes of conventional LVTSCRs form part of the prior art.

Claim 4, it is respectfully submitted, does not lack definiteness. The "desired" elevated holding voltage is the predetermined voltage chosen by the manufacturer to avoid latch-up. In the specification one such "desired" voltage is given as a voltage that is above the DC bias, e.g. the power supply voltage, to avoid latch-up (page 5, second last paragraph and page 11, lines 4-6). The critical size for the second region (region 316) is determined by TCAD simulations as discussed on page 9, first two lines. Thus the specification clearly explains how the size is chosen using TCAD simulations to achieve a holding voltage that avoids latch-up. Thus both the desired voltage and the manner of achieving it are clearly defined.

Claims 5 and 6 depend from claim 4 and therefore include the same limitations and are therefore also sufficiently definite in terms of 35 USC 112.

Claim 7, it is respectfully submitted, also does not lack definiteness. As explained above with respect to Claim 4, the desired level of the holding voltage is clearly defined as being a level that avoids latch-up. For instance it is a voltage that is above the DC bias. This is determined by TCAD simulations. Thus the "desired" holding voltage is clearly defined as a level that avoids latch-up (which depends on the application in which the device is to be used, and can be clearly determined), and the amount of reduction in size is clearly determinable by TCAD simulations. Thus reducing the size "sufficiently" so as to increase the holding voltage to the "desired level" is clearly defined in the specification and does not lack definiteness under 35 USC 112.

Claim 8, it is respectfully submitted, also does not lack definiteness. As explained above with respect to Claim 7, the desired level of the holding voltage is clearly defined as being a level that avoids latch-up. For instance it is a voltage that is above the DC bias. Also, as explained on page 8, last two lines, to page 9, first two lines: increasing n+emitter 322 has a beneficial effect if p+ emitter 316 is reduced below a critical size, as can be determined by simulation techniques. The invention therefore clearly states the method involved in choosing the sizes of the two regions 332, 316, and contemplates that this be done using TCAD simulations in order to identify the appropriate sizes where holding voltage is high enough to avoid latch-up. By manipulating the p+ emitter 316 below the size of a conventional LVTSCR and increasing the size of the n+emitter 322, the desired holding voltage can be achieved. It will be appreciated that there is no single correct set of sizes – variations of both of the two regions will effect the holding voltage, and manipulation of the two sizes using TCAD simulations is used in accordance with the described method of the invention. The "desired" holding voltage is clearly defined as a level that avoids latch-up (which depends on the application in which the device is to be used, and can be clearly determined), and the amount of reduction in size of the p+ emitter and increase in size of the n+emitter is clearly determinable by TCAD simulations. Thus, the size changes of the two regions so as to increase the holding voltage to the "desired level" is clearly defined in the specification and does not lack definiteness under 35 USC 112.

Claim 9 has been amended in order to simplify the language. The deleted wording merely sought to describe the internal mechanism involved in achieving the increase in holding voltage. Since this is not relevant to the structural details of the device, the claim has been amended to include only structural details necessary to achieve the desired result. It is respectfully submitted that Claim 9 as previously claimed and as now amended is not indefinite under 35 USC 112. As explained above with respect to Claim 7, the desired level of the holding voltage is clearly defined as being a level that avoids latch-up. For instance it is a voltage that is

above the DC bias. This is determined by TCAD simulations. Thus the "desired" holding voltage is clearly defined as a level that avoids latch-up (which depends on the application in which the device is to be used, and can be clearly determined), and the amount of reduction in size is clearly determinable by TCAD simulations. Thus reducing the size "sufficiently" so as to increase the holding voltage to the "desired level" is clearly defined in the specification and does not lack definiteness under 35 USC 112.

Claim 10, it is respectfully submitted, also does not lack definiteness. As explained above with respect to Claim 8, the desired level of the holding voltage is clearly defined as being a level that avoids latch-up. For instance it is a voltage that is above the DC bias. Also, as explained on page 8, last two lines, to page 9, first two lines: increasing n+emitter 322 has a beneficial effect if p+ emitter 316 is reduced below a critical size, as can be determined by simulation techniques. The invention therefore clearly states the method involved in choosing the sizes of the two regions 332, 316, and contemplates that this be done using TCAD simulations in order to identify the appropriate sizes where holding voltage is high enough to avoid latch-up. By manipulating the p+ emitter 316 below the size of a conventional LVTSCR and increasing the size of the n+emitter 322, the desired holding voltage can be achieved. It will be appreciated that there is no single correct set of sizes – variations of both of the two regions will effect the holding voltage, and manipulation of the two sizes using TCAD simulations is used in accordance with the described method of the invention. The "desired" holding voltage is clearly defined as a level that avoids latch-up (which depends on the application in which the device is to be used, and can be clearly determined), and the amount of reduction in size of the p+ emitter and increase in size of the n+emitter is clearly determinable by TCAD simulations. Thus, the size changes of the two regions so as to increase the holding voltage to the "desired level" is clearly defined in the specification and does not lack definiteness under 35 USC 112.

Rejection under 35 USC 102/103(a):

Claims 1-10 are distinguishable over prior art Figures 1and 2 since all of the claims include the limitation of reducing the size of the second region.

The size reduction in claims 1-3 is such as to provide a region that is smaller than that in the prior art. Thus it specifically distinguishes over the prior art (Figures 1 and 2).

Claims 4-7, 9 specify the size reduction to be such as to increase holding voltage to a desired level (claims 4-7). The desired level is discussed above as relating to a level that avoids latch-up. The prior art, specifically suffers from the problem of latch-up. Thus the present claims 4-7 specify a decrease in size of the second region which ensures that latch-up is avoided for the particular application. This is not contemplated by the prior art (Figures 1 and 2). Therefore the prior art neither teaches nor suggests such a change in the size of the second region.

Claims 8 and 10 specify reducing p+ emitter below a predetermined size and increasing n+emitter to increase holding voltage to the desired value. Again, the desired level is discussed above as relating to a level that avoids latch-up. The prior art, specifically suffers from the problem of latch-up. Thus claims 8 and 9 specify a decrease in size of the p+ emitter region and increase in size of the n+ emitter region which ensures that latch-up is avoided for the particular application. This is not contemplated by the prior art. Therefore the prior art neither teaches nor suggests such a change in the dimensions of these two regions.

New Claims

New claims 11-18 have been included to highlight the manner in which ESD protection structures of the invention are made with the desired parameters by adjusting the p+ and optionally the n+ emitter regions.

It is respectfully submitted that the claims as they now stand (claims 1 – 20) are definite under 35 USC 112 and are novel and non-obvious over the prior art. It is therefore respectfully requested that the claims 1-20 be permitted to proceed to allowance.

Version with markings to show changes made:

1. (Amended) A device formed in a semiconductor material of a first conductivity type, the semiconductor material having a dopant concentration, the device comprising:
   a well of a second conductivity type formed in the semiconductor material, the well having a dopant concentration;
   a first region of the second conductivity type formed in the well, the first region having a dopant concentration greater than the dopant concentration of the well, the first region being connected to a first node;
   a second region of the first conductivity type formed in the well, the second region having a dopant concentration greater than the dopant concentration of the semiconductor material, the second region being connected to the first node;
   a third region of the second conductivity type formed in the semicondúctor material, the third region having a dopant concentration greater than the dopant concentration of the well, the third region being connected to a second node, and
   a fourth region of the first conductivity type formed in the semiconductor material, the fourth region having a dopant concentration greater than the dopant concentration of the semiconductor material, the fourth region being connected to the second node, wherein the second region is reduced in size (to reduce the number of minority carrier that are injected to at least a point where holding voltage is increased beyond the holding voltage of) compared to a conventional LVTSCR of the same process.

3. (Amended) The device of claim 2, wherein the third region is increased in size relative to that of a conventional LVTSCR of the same process, to reduce space charge neutralization.

9. (Amended) A method of providing a device having a higher holding voltage than a LVTSCR and supporting a higher current than a GGNMOS, comprising providing a LVTSCR-like structure having a p+ emitter that is sufficiently reduced in size so as to (limit hole injection to the point where the space charge neutralization is so limited as to) increase the holding voltage to a (the) desired level.

Respectfully Submitted,

Dated: 9/22, 2002

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